IN THE ABSTRACT:

Please delete the Abstract in its entirety and replace with the following:

--**ABSTRACT**

A content addressable memory comprises a CAM control logic unit and plural cells connected in a chain. Each cell comprises a memory block coupled to a common address bus, a comparator coupled to a common data bus and to the data interface of the memory block. A switch couples the data interface of the memory block with the data bus, and a logic block including a Match flip-flop. The memory is operable in a Search phase and an Access phase. In the Search phase, a sequence of words on the common data bus is serially matched with the contents of a sequence of addresses in the memory blocks. In the Access phase, the cells matched in the Search phase are made serially available for access via the common address and data buses.--